Eng. Sci., 2025, **38**, 1906

Engineered Science
DOI: https://dx.doi.org/10.30919/es1906

$Ti_3C_2T_x$ -MXene Based Planar Memristors on Flexible Cyclic Olefin Copolymer with Voltage-Controlled Switching Behavior for Neuromorphic Applications

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Abstract

Real-time edge artificial intelligence (AI) demands memory elements that are not only energy-efficient and multifunctional, but also compact, tunable, and integrable with flexible substrates. Planar memory architecture offers distinct advantages for neuromorphic computing, including surface accessibility, facile fabrication, and seamless integration with flexible substrates, making it ideal for next-generation synaptic hardware. Traditional metal oxide-based memristors often fail to meet all these requirements simultaneously due to their rigid architecture and limited material versatility. Herein, we present a planar $Ti_3C_2T_x$-MXene-based memristor (PMX-memristor) fabricated on a flexible cyclic olefin copolymer (COC) substrate, constituting the first fully planar MXene-based resistive device reported to date. The planar architecture exposes the active MXene channel, which enables direct surface inspection and functionalization while delivering robust analog switching. By tuning the voltage amplitude, the device operates in two modes: (i) a volatile regime based on valence change dynamics with transient conductance states, and (ii) a non-volatile regime driven by voltage-induced Ti→TiOx transformation, supporting eight distinct resistance levels. Detailed EDX and XPS analyses, performed before and after electrical stress, confirm the voltage-induced oxidation pathway that underpins this dual-mode behavior. The memristor's eight-level precision enables compact 9-bit weight encoding using 3×3-bit multi-level cells in crossbar arrays, reducing area and energy compared to binary implementations. We demonstrate end-to-end deployment of these devices in spiking neural networks for real-time classification of neuromorphic vision datasets, showcasing high-performance, task-relevant learning capabilities on benchmarks such as N-MNIST and DVS-Gesture. These results underscore the potential of the designed PMX-memristor for voltage-controlled, neuromorphic edge computing and provide direct surface accessibility for functionalization and potential bio-interfacing for next-generation smart wearables.

Keywords: MXene memristor; Multistate analog switching; Neuromorphic computing; Volatile/non-volatile switching.
Received: 10 July 2025; Revised: 30 September 2025; Accepted: 24 November 2025
Article type: Research article.

1. Introduction

As AI increasingly shifts toward real-time edge computing, there is a critical demand for memory technologies that can emulate biological synapses with high accuracy, power efficiency, and fabrication scalability. Conventional vertical-stacked memory architectures often struggle to meet these demands, particularly when flexibility, multifunctionality, and integration with emerging substrates are required.[1] Planar memory devices have recently gained attention for neuromorphic applications due to their unique structural advantages, including surface accessibility, simplified fabrication, and compatibility with flexible and transparent substrates. These features make planar architecture particularly attractive for building efficient, integrable, and reconfigurable neuromorphic systems. Traditional memory technologies, such as Flash and DRAM, are constrained by Moore's Law and suffer from significant energy inefficiencies in modern computing paradigms.[2] Alternatively, memristor-based memory technologies offer non-volatility, high density, and the potential for energy- efficient in-memory computation,

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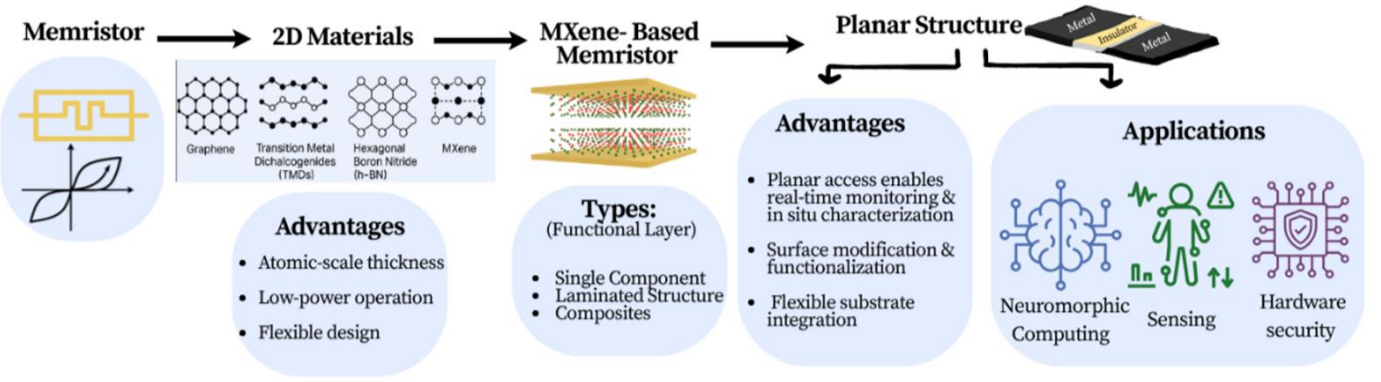

Fig. 1: Schematic overview of MXene-based planar memristors in emerging memory technologies. Transition from conventional memristors to 2D-material-based architectures, emphasizing planar MXene designs and their advantages for neuromorphic computing, sensing, and hardware security.

making them strong candidates for next-generation computing architectures.[3] Moreover, their ability to store multiple resistance states enables neuromorphic architectures,[4] further enhancing their relevance in AI and edge computing.[5] In such systems, memristors can emulate key synaptic behaviors such as potentiation, depression, and spike timing-dependent plasticity, allowing for real-time learning, parallel information processing, and energy-efficient computation in hardware-based neural networks. Memristors have also demonstrated potential in biosensing for label-free cancer biomarker detection due to their sensitivity and compact size,[6,7] as well as in hardware security through applications like physical unclonable functions and random number generation, enabled by their device-level variability.[8]

While early memristor research focused heavily on metal oxide materials such as TiO_2,[9] ZnO,[10] HfO_2,[11] ZrO_2,[12] Ta_2O_3,[13] Al_2O_3,[14] and CuO.[15] These systems often face challenges related to variability, scalability, and limited tunability due to their rigid architecture and limited material versatility.[16] In contrast, the emergence of two-dimensional (2D) materials has opened new pathways for memory and electronic devices due to their unique electronic properties, mechanical flexibility, and high surface-to-volume ratio. Among these, transition metal carbides and nitrides, known as MXenes, have attracted significant attention for their outstanding electrical conductivity, tunable surface chemistry, and solution-processable nature.[17] Unlike traditional 2D materials such as graphene and transition metal dichalcogenides (TMDCs), MXenes offer intrinsic metallic conductivity combined with hydrophilic functional groups (-OH, -O, -F), which enable stable resistive switching for memristor applications.[18] These materials also demonstrate excellent environmental stability, making them ideal for long-term, energy-efficient memory storage and neuromorphic computing.[19] The ability of MXene-based devices to sustain high mechanical flexibility further expands their potential for integration into wearable and implantable electronics, overcoming the limitations of conventional memory materials.[20] The performance of memristors is generally assessed using parameters such as switching thresholds (V_{set}/V_{reset}), ON/OFF resistance ratio, retention time, and endurance under repeated cycling. For neuromorphic and analog applications, additional emphasis is placed on the ability to achieve multiple, stable conductance states with good separability and reproducibility. These benchmarks provide a common basis for comparing different material systems and architectures, and frame the improvements reported in MXene-based devices. A hierarchical roadmap that situates planar MXene memristors within the broader landscape of emerging memory technologies is illustrated in Fig. 1.

Recent advancements in MXene-based memristors have explored a range of device architectures and material combinations, including laminated structures and hybrid composites. These approaches often integrate MXenes with other functional materials such as ZnO, TiO_2, ferroelectrics, or polymers to enhance switching stability, transparency, and mechanical flexibility.[21-24] While these multilayered or composite systems have shown promising results, such as improved endurance, reduced SET voltages, and emulation of synaptic dynamics, they introduce fabrication complexity and can obscure the origin of the switching behavior, making it difficult to isolate the role of MXene itself. Moreover, variations in interface properties and interlayer dynamics can lead to increased variability and reduced reproducibility across devices. In contrast, devices utilizing MXene as a standalone switching layer offer distinct advantages in terms of fabrication simplicity, structural uniformity, and interpretability of switching mechanisms. Thin films composed solely of $Ti_3C_2T_x$ MXene have demonstrated

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reliable multistate resistive switching, long retention, low operating voltages, and high ON/OFF ratios.[25-27] These characteristics are particularly beneficial for low-power memory applications, where device performance can be more directly attributed to the inherent properties of the MXene itself, such as oxygen vacancy migration and surface terminations, without interference from additional material layers. The use of single-component MXene devices also supports the broader goal of developing simpler, more scalable alternatives to traditional metal oxide-based memristors, offering a cleaner pathway toward compact, energy-efficient, and neuromorphic-compatible memory technologies. Despite the promising properties demonstrated in previously reported MXene-based memristors using standalone switching layers, their integration into planar device architectures remains largely unexplored. This gap limits the development of lateral architectures capable of combining low-power memory and neuromorphic functionality with surface accessible features such as sensing and functionalization. Furthermore, there is a scarcity of analog memristive devices that can reliably achieve many distinct and stable resistance states, an essential requirement for efficient synaptic emulation and multilevel memory applications.

Recent MXene memristors have primarily been demonstrated in vertical metal-insulator-metal stacks or composite multilayers, where additional oxide, polymer, or ferroelectric components improve stability but obscure the intrinsic role of MXene and complicate fabrication.[21-24] Stand-alone $Ti_3C_2T_x$ layers in MIM devices show promising retention and endurance,[25-27] yet they remain confined to out-of-plane geometries with limited surface accessibility. By contrast, planar 2D memristors reported with CNTs[28] and graphene[29] achieve multilevel operation but typically require higher voltages and do not exhibit voltage-tunable volatile/non-volatile transitions. In this context, the presented fully planar Au/$Ti_3C_2T_x$/Au device on a flexible cyclic olefin copolymer (COC) substrate is distinct as it combines low switching voltages with eight reproducible analog states, exposes the channel surface for in-situ functionalization, and uniquely supports bias-controlled dual-mode operation. Beyond our work, COC has already found broad use in microfluidics and microsystems due to its low water uptake, chemical stability, and biocompatibility,[30] and, more recently, as a piezoelectret material with excellent piezoelectric and thermal-mechanical properties.[31] Such multifunctionality underscores its value as a substrate for next-generation electronic and sensing devices, further reinforcing its relevance for our planar MXene platform.

In this work, we present a PMX-memristor device, fabricated on a flexible COC substrate. Unlike the conventional vertical MIM geometry commonly found in the literature, our planar configuration exposes the active switching layer, enabling direct surface access for in situ characterization, surface functionalization, and potential biosensing integration. This geometry also simplifies fabrication, supports optical probing, and aligns well with CMOS-compatible processing. The device exhibits robust multistate resistive switching behavior, with clearly defined and reproducible resistance levels. Most notably, by varying the operating bias conditions, the device demonstrates a tunable transition between volatile and non-volatile switching modes, which is a valuable trait in MXene-based systems. This dual-mode operation offers significant potential for reconfigurable memory, neuromorphic computing, and adaptive sensing platforms. By leveraging the inherent electrical properties of MXene and the multifunctionality of a planar layout, this work advances the development of next-generation memory, sensing and neuromorphic architectures with configurable operation and simplified planar design for smart wearable technology.

2. Experimental methods

2.1 Materials

All chemicals and reagents used in this study were of analytical grade and utilized as received without any additional purification. Deionized water (18.2 MΩ·cm), obtained from a Milli-Q water purification system, was used for the preparation of all aqueous solutions and dispersions.

2.2 Synthesis of 2D Ti_3C_2Tx MXene sheets (TMS)

The delaminated 2D $Ti_3C_2T_x$ MXene nanosheets (TMS) were synthesized using a Modified-MILD protocol. Commercially available Ti_3AlC_2 MAX-phase powder (~40 μm; Carbon-Ukraine Ltd.) was used as the precursor. Initially, a 15 mL solution of 9 M hydrochloric acid (HCl, 37% w/w; VWR International) was prepared and maintained at 40 °C under continuous magnetic stirring at 500 rpm. Subsequently, 1.4 g of lithium fluoride (LiF, <100 μm, ≥99.98%, Merck Millipore) was gradually added to the acidic solution and stirred for ~15 min, resulting in a transparent solution. In the next step, 600 mg of Ti_3AlC_2 powder was slowly introduced into the etching solution. The reaction mixture was stirred vigorously at ambient temperature for 24 h to selectively remove the Al atomic layers, facilitating the formation of 2D layered $Ti_3C_2T_x$ sheets. The obtained dispersion was subjected to 5-7 washing cycles using ultrapure DI water and centrifugation at 6000 rpm for 8 min per cycle, until the supernatant reached a neutral pH. The exfoliated product was collected by performing a final centrifugation at 3800 rpm for 15 min. The loosely aggregated TMS were redispersed by gentle agitation, forming a stable colloidal suspension with an Ebony color. The concentration of the as-prepared TMS dispersion was estimated to be approximately 15±5 mg·mL^{-1} by determining the mass of a vacuum-filtered film obtained from a known volume of the dispersion.

2.3 Materials characterization and device testing

A field-emission scanning electron microscope (FEG-SEM, JEOL JSM-7610F, Japan), equipped with an energy-dispersive X-ray spectroscopy (EDX) detector, was used for detailed

morphological analysis, nanoscale features, and elemental composition mapping of the prepared samples. High-resolution imaging was further conducted via transmission electron microscopy (TEM, FEI Titan G2 80-300 ST, Thermo Fisher Scientific) at 200 kV. For TEM analysis, a diluted suspension of the TMS was drop-cast onto lacey carbon-coated copper grids and dried under ambient conditions. To investigate the crystalline structure and phase composition, X-ray diffraction (XRD) measurements were carried out using a Bruker D8 Advance X-ray diffractometer equipped with Cu-Kα radiation (λ = 1.5406 Å). The operating conditions were set to a current of 15 mA and a voltage of 40 kV. The surface chemical composition and oxidation states of elements were analyzed using X-ray photoelectron spectroscopy (XPS, Escalab 250Xi, Thermo Scientific, USA), employing Al-Kα radiation as the excitation source. Atomic force microscopy (AFM) measurements were performed in tapping mode using an MFP-3D Origin Plus system (Asylum Research, Oxford Instruments, USA), equipped with Au-coated silicon cantilevers (Tap300GB-G, Budget Sensors; spring constant ≈ 40 $N \cdot m^{-1}$). A thin layer of diluted TMS dispersion was deposited onto a silicon substrate to assess the 2D nanosheet thickness with high precision. Laser exposure during device fabrication was performed using the Dilase laser patterning system. Electrical measurements were carried out using a Keithley 4200 Parameter Analyzer (Tektronix, USA) to characterize the device's electrical performance. The system was operated with its proprietary software to perform current-voltage (I-V) measurements and other electrical analyses.

2.4 Device fabrication

PMX-memristor devices were fabricated using a standard photolithographic lift-off process, as illustrated in Fig. 2g. A uniform TMS film was first formed by spin-coating a 2 $mg \cdot mL^{-1}$ ethanol-based dispersion onto a pre-cleaned substrate, followed by soft baking at 100 °C for 5 minutes to ensure solvent evaporation and film adhesion. Subsequently, a thin gold layer was deposited over the 2D TMS film via sputtering, serving as the electrode material. A positive-tone photoresist was then applied and patterned using direct-write laser lithography (Dilase system) to define the electrode geometry. After development, the exposed regions of the gold layer were selectively removed by wet etching, and the residual photoresist was stripped using acetone. This process yielded PMX-devices in which a 2D TMS channel bridges the patterned gold electrodes with lateral separation, forming the active region of the memristor. The resulting architecture combines material simplicity with precise dimensional control, offering a scalable route for lateral MXene-based memory elements.

3. Results and discussion

3.1 Structural and morphological analysis of 2D TMS

The rise of 2D materials has sparked significant advancements in electronic and memory device architectures for next-generation neuromorphic and in-memory computing systems. Among emerging 2D materials, TMS is a leading candidate for resistive memory and analog switching due to its high in-plane conductivity, tunable surface terminations, and solution-processable handling with flexible architecture. The prepared TMS 2D sheets geometry allows for close contact with electrodes in planar devices, and their surface-rich chemistry enables dynamic manipulation of electrical characteristics. Benefiting from these characteristic features, we fabricated and characterized the PMX-memristors, which demonstrated voltage-tunable behavior, transitioning from volatile to non-volatile modes. We started with the synthesis of 2D TMS that involved selective chemical etching of the Al atomic layer from the Ti_3AlC_2 MAX-phase, followed by delamination, yielding high-quality 2D TMS dispersed in water (see Fig. 2a). SEM analysis (Fig. 2b and 2c) reveals a clear transformation from the multilayered, stacked morphology of the parent MAX phase to a homogeneous, 2D sheet-like structure with lateral dimensions of a few ~2-5 microns. The successful delamination of TMS is further confirmed by TEM imaging (Fig. 2d), where ultrathin, semi-transparent nanosheets are observed, typical of few-layer 2D materials. Atomic force microscopy (AFM) was employed to assess the thickness and surface morphology of individual $Ti_3C_2T_x$ MXene nanosheets. As shown in Fig. 2e, the topographic analysis revealed an average flake thickness of approximately ~2.5 nm, indicative of few-layer exfoliation. This nanoscale thickness confirms the successful delamination of the Ti_3AlC_2 MAX phase into high-quality 2D TMS, essential for achieving efficient charge transport in planar device architectures. To evaluate the phase purity and structural transformation from the MAX precursor to the final 2D TMS product, X-ray diffraction (XRD) measurements were conducted. The diffraction pattern of the Ti_3AlC_2 precursor (Fig. 2f) matches well with JCPDS 52-0875, showing well-defined peaks characteristic of the layered MAX structure. In contrast, the XRD profile of the exfoliated TMS exhibited the disappearance of the Al-related peak at $2\theta \approx 38.9°$, confirming the successful etching of the Al layer. Furthermore, the (002) reflection undergoes a notable downshift from $2\theta \approx 9.87°$ in the MAX phase to $2\theta \approx 6.90°$ in the exfoliated TMS, accompanied by peak broadening and intensity reduction. This shift reflected an increase in interlayer spacing due to surface functionalization and water intercalation during the etching and delamination process, further verifying the formation of few-layer TMS with expanded lamellar structure. These findings confirmed the effectiveness of the synthesis protocol in producing phase-pure, delaminated TMS suitable for device integration. The fabrication workflow of the planar memristor is illustrated in Fig. 2g, involving sequential spin coating of TMS at 1000 rpm to achieve an active layer of ≈ 100 nm, Au sputtering as an electrode, and photolithographic patterning via UV exposure and wet etching. The chosen spin-coating parameters and active layer thickness were informed by a recent study optimizing the deposition conditions of 2D TMS on COC

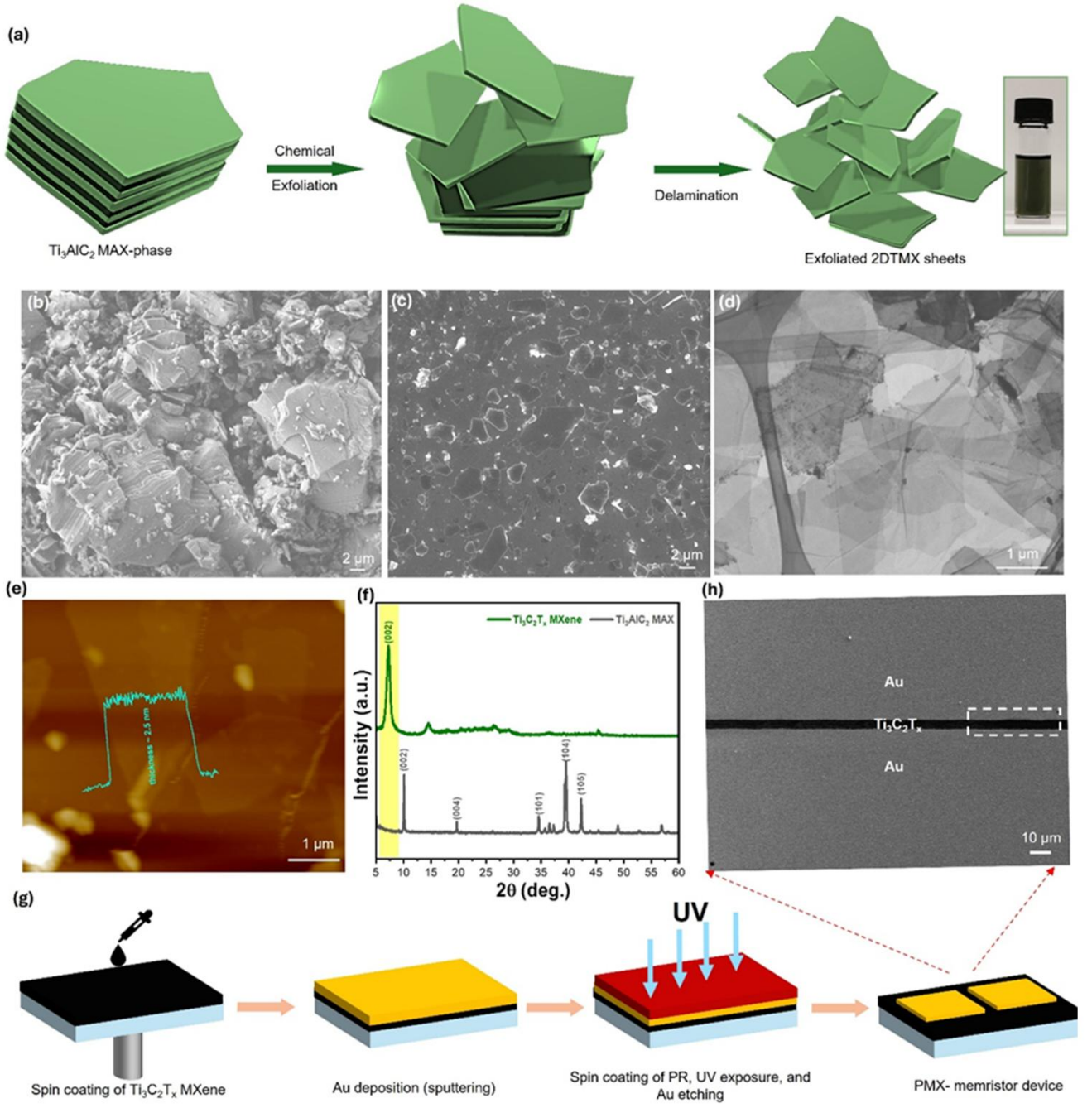

Fig. 2: Structural and morphological characterization of 2D-TMS and device fabrication. (a) Schematic of 2D-TMS chemical synthesis; the inset is a digital photograph of the 2D-TMS aqueous ink. (b) SEM image of bulk Ti_3AlC_2 MAX powder. (c) SEM image of delaminated 2D-TMS flakes. (d) TEM image shows exfoliated 2D TMS thin sheets. (e) AFM height profile. (f) XRD patterns of MAX phase and the synthesized exfoliated 2D-TMS. (g) Schematic of planar PMX-memristor device fabrication. (h) SEM image exhibits the device configuration.

substrates.[32] To determine the optimal electrode spacing, we initially fabricated and tested devices with gap sizes ranging from 40 µm to 115 µm. As shown in Fig. S1, we observed that reducing the gap size led to a marked increase in the RON/ROFF ratio. Based on this trend, we selected the smallest reliably achievable gap within the limits of our photolithography setup, which was 10 µm. The SEM image in Fig. 2h shows a top-view of the final Au-TMS-Au planar architecture, with a clearly defined 2D TMS channel bridging the two electrodes. This lateral geometry provides direct access to the active switching layer, enabling electrical, optical, and surface-based functionalization.

3.2 Multi - state analog switching behavior

To study the resistive switching characteristics of the fabricated PMX-memristor device, a comprehensive set of voltage sweep, and pulse-based electrical measurements were performed. These tests systematically probed the device's dynamic switching behavior and capacity for stable multistate memory operation. Initially, Typical I-V sweeps of the PMX

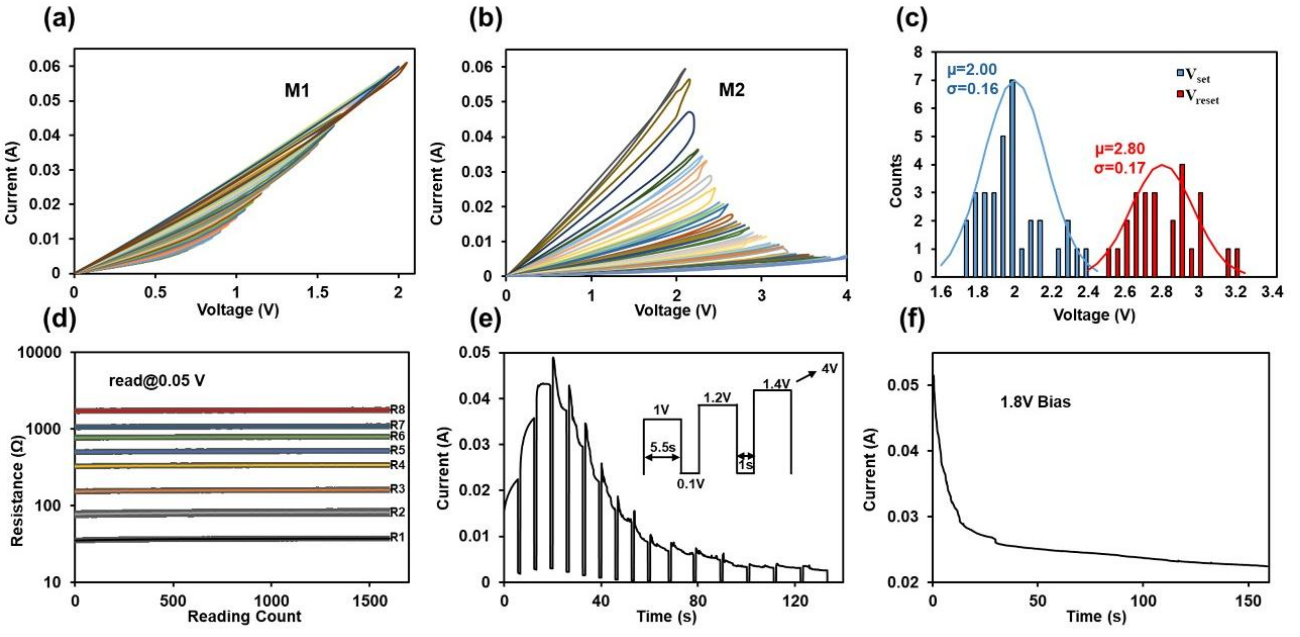

Fig. 3: Comprehensive analysis of resistive switching and multistate behavior in PMX-memristors. (a) Multistate behavior where current increases with each voltage sweep (M1). (b) Multistate behavior where current begins to decline with increasing voltage (M2). (c) Statistical distribution of Vset and Vreset across 35 fresh devices. (d) Eight programmable resistance states averaged from three devices each, with standard deviation indicated as shaded boundaries. (e) Current modulation using voltage pulses from 1 V to 4 V, revealing M1/M2 switching behavior. (f) Demonstration of broad current range coverage using a constant 1.8 V bias, showing application-relevant programmability.

device is shown in Fig. S2. On applying the voltage sweep of 1.6V, the device undergoes a resistive switching loop between the high-resistance state (HRS) and low-resistance state (LRS). In the second sweep of 2.6V, the device starts with its initial resistance and switches to a significantly higher resistance (OFF state). The fact that the second sweep started from the device's initial resistance indicates that it reset, which suggests temporary retention (volatile behavior). Fig. 3 presents a detailed evaluation of the device's performance, highlighting its dual-mode response, performance consistency, and the realization of multiple discrete resistance levels. The multistate characteristics of the device were explored as shown in Fig. 3a-b, where two distinct operational modes are evident: Mode 1 (M1), where current increases with each voltage sweep, and Mode 2 (M2), where current begins to decline with increasing voltage. In M1, the I-V sweeps in Fig. 3a overlap slightly, meaning each new ramp starts before the device has fully relaxed to its original high-resistance state. The brief pause leaves residual mobile species in the $Ti_3C_2T_x$ layer, so every subsequent trace begins from an intermediate resistance. This behavior confirms the volatile, self-resetting character of M1 and indicates that the resistance baseline can be tuned by simply adjusting the relaxation interval between sweeps.

In M2, each subsequent sweep begins from the resistance state attained at the end of the previous cycle, without resetting to the original value, clearly demonstrating non-volatile switching behavior in this regime. Statistical analysis from 35 freshly fabricated devices outlining set voltage (V_{set}) and reset voltage (V_{reset}) shows consistent switching as shown in Fig. 3c. V_{set} corresponds to the point at which the device reaches its lowest resistance, while V_{reset} is defined as the voltage at which current falls below 0.02 A, indicating that the device has fully transitioned to the OFF state. Devices follow a normal distribution with an acceptable standard deviation. The switching point between M1 and M2 behavior aligns with the V_{set}, indicating a critical transition voltage for state modulation. Further, validating the multistate operation, Fig. 3d displays eight distinct resistance states achieved through repeated programming. To program each resistance state shown, a voltage sweep of increasing amplitude was applied to the device to write the desired state, followed by a series of read pulses at 50 mV to monitor the resistance over time. This write-read cycle was repeated sequentially for each state, with the resulting traces in the plot representing the resistance evolution at 50 mV for each programmed level. Each trace represents the average of three devices, and the shaded region around each curve reflects the standard deviation, demonstrating both reproducibility and variance tolerance across devices. Write pulses ranging from 1 V to 4 V (5.5 s pulse width) in 0.2 V steps were applied, followed by a read pulse of 0.1 V (1 s pulse width) to observe the full current window of the device, as shown in Fig. 3e. The resulting current levels reveal clear multistate transitions and M1/M2 dynamics. In Fig. 3f, a constant bias of 1.8 V was applied to the device for an extended duration to assess its capacity for analog tuning under fixed-voltage operation. This approach was able to traverse a wide portion of the dynamic current

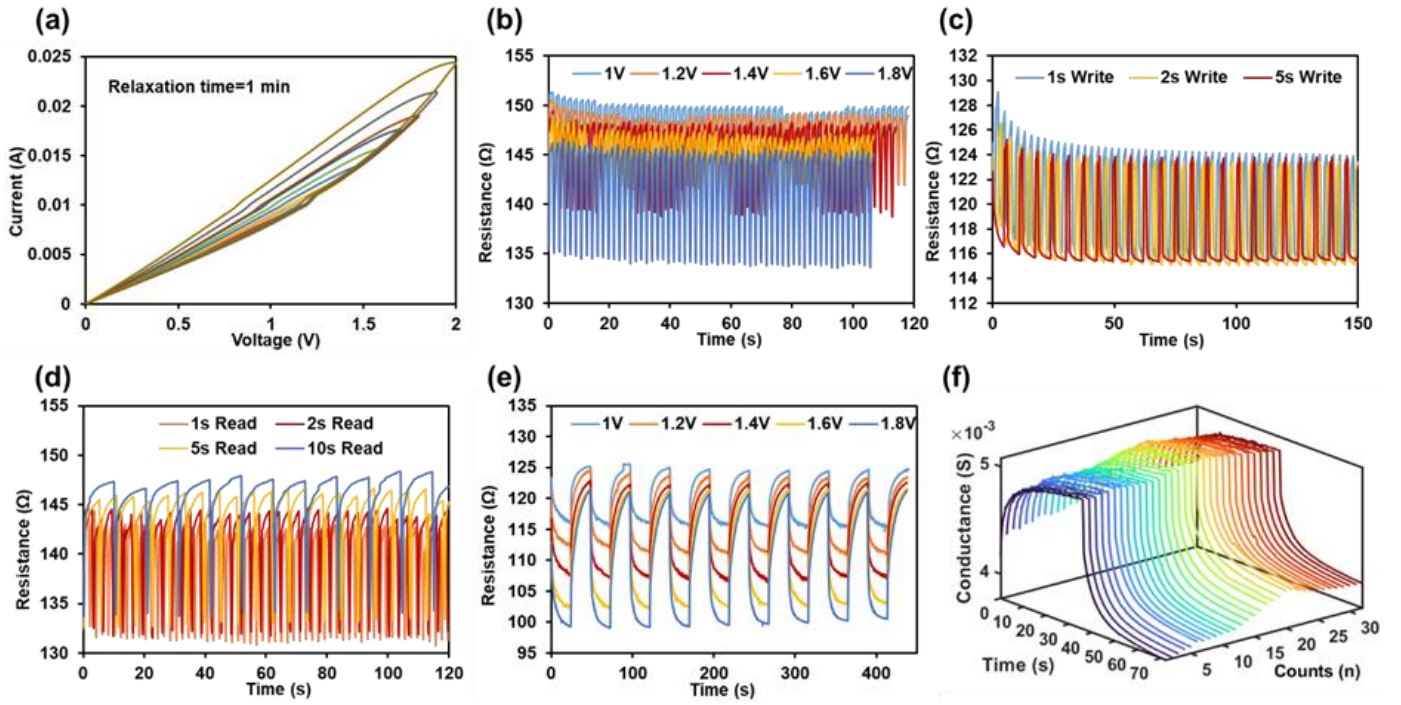

Fig. 4: Dynamic and volatile switching behavior of PMX-memristors under varying sweep and pulse conditions. (a) Successive voltage sweeps below Vset show consistent ON switching followed by self-resetting behavior, indicating volatile operation. (b) Resistance modulation as a function of write pulse amplitude (1.0 V-1.8 V). (c) Effect of varying write pulse width at fixed amplitude (1.8 V) showing minimal dependence on duration. (d) Resistance recovery behavior under varying read pulse widths. (e) Potentiation and depression curves under different write amplitudes. (f) Conductance stability over 30 consecutive write-read cycles at 1.8 V.

range previously accessed via the pulsed method, indicating that complex pulse programming may not be essential for exploiting the device's multilevel storage capabilities. This finding is particularly significant from a systems integration perspective, as it suggests that simple, fixed voltage driving schemes can be employed in practical circuit implementations while still leveraging the device's rich multistate behavior.

To further explore the volatility observed in Mode 1 (M1) and assess the dynamic response of the memristive behavior, a series of sweep and pulse-based experiments were conducted, as illustrated in Fig. 4. In Fig. 4a, a fresh PMX-device was subjected to consecutive voltage sweeps with incrementally increasing amplitudes, each separated by a 1-minute relaxation period. The results consistently show that the device transitions from the HRS to the LRS during each sweep (ON switching) but then reverts to its original resistance before the next sweep begins. This repeatable self-resetting behavior confirms the volatile nature of the switching in M1, where the device does not retain its conductance once the stimulus is removed, highlighting its potential for transient sensing or short-term synaptic memory applications. Next, the influence of write pulse amplitude on resistive switching was investigated, as shown in Fig. 4b. Pulses with increasing voltage (1.0 V to 1.8 V) were applied while maintaining fixed write and read durations of 2 s each. The device displays pronounced resistance modulation at higher amplitudes, particularly at 1.8 V, where a stronger contrast between HRS and LRS is observed. This behavior indicates that higher voltage amplitudes promote more substantial formation of oxygen vacancies and localized reduction of Ti ions, resulting in deeper modulation of conductance. These results highlight the amplitude-dependent nature of switching in the volatile regime and demonstrate a simple means to tune the device's transient response. To explore the temporal sensitivity of the device to stimulus duration, the write pulse width was varied in Fig. 4c, while maintaining a constant write amplitude of 1.8 V and a fixed read pulse (2 s at 0.05 V). Each cycle shows a clear drop in resistance during the write pulse and a recovery back to the original state during the read phase, again confirming the volatile nature of switching. However, variation in write duration produced only modest differences in resistance modulation, suggesting that the filamentary processes or local redox activity responsible for switching occur rapidly and are primarily voltage-driven rather than time-dependent. Similarly, the effect of read pulse duration was assessed in Fig. 4d, with write parameters held constant. The device continues to display reversible switching, with minimal variation introduced by changes in read duration. The consistent recovery behavior across all conditions further supports the notion that the self-resetting mechanism is intrinsic to the material system and not significantly affected by read pulse timing. The potentiation and depression behavior under varying voltage levels is explored in Fig. 4e. Here, alternating write and read pulses (every 25 s) at multiple amplitudes simulate synaptic weight adjustment. The results reveal a clear analog modulation of conductance over time,

mimicking gradual learning behavior in artificial synapses. Notably, the degree of modulation and relaxation dynamics vary with applied voltage, highlighting the tunability of synaptic plasticity features in the PMX-memristors through simple voltage control. Finally, the repeatability and stability of the volatile switching mode were assessed through repeated write-read cycles at a fixed voltage of 1.8 V for 30 cycles, as shown in Fig. 4f. The conductance remained stable with minimal degradation or drift over time, demonstrating excellent device stability and repeatability. This confirms the robustness of the volatile switching mechanism for use in short-term memory and dynamic sensing applications. Collectively, the results in Fig. 4 offer a comprehensive understanding of the temporal dynamics and volatility of the PMX-memristors in M1 operation. The ability to exhibit reliable, reversible, and amplitude-tunable switching positions these devices as promising candidates for short-term memory, adaptive sensing, and volatile neuromorphic computing systems. Mechanical reliability under cyclic bending was also evaluated. The sheet resistance was recorded while the flexible device underwent bending around a Mayer rod with a 9.5 mm radius for up to 1000 cycles (Fig. S3). The initial resistance of roughly 26 kΩ increased gradually to about 31 kΩ after the full test, corresponding to a modest ~ 20 % change. This limited change confirms that the $Ti_3C_2T_x$ layer and its adhesion to the COC substrate remain intact under repeated bending, highlighting the suitability of the PMX-memristor for wearable and other mechanically dynamic applications.

3.3 Proposed switching mechanism

The performance of the fabricated PMX device is linked to the 2D morphological and chemical characteristics of the TMS. The planar geometry ensures that the electric field is applied laterally across the TMS channel, directly engaging the surface and edge terminations (-OH, -O, -F). These terminations, known to influence surface conductivity and defect dynamics, play a dual role to modulate ionic mobility and function as reactive sites for electrochemical transformations under bias voltage. At low bias voltage, valence change memory is dominant, where conductance modulation is governed by reversible field-induced modulation of charge distribution within the TMS layer or at its interfaces due to termination groups, while layered morphology facilitates fast relaxation and low retention. This corresponds to the volatile regime (Mode 1), where conductance states reset upon stimulus removal. In this regime, filament formation and rupture occur dynamically when power is switched on and off, resulting in reproducible ON/OFF switching cycles. This process is fully reversible, and the device consistently resets to its initial state after stimulus removal, maintaining low retention and volatile switching as shown in Fig. 5a and 5b. As the applied voltage increases beyond the set voltage ~2 V (M2), the localized Joule heating and electric field strength become sufficient to trigger edge-site oxidation and structural distortion due to the formation of $Ti \rightarrow TiO_x$ clusters as indicated in Fig. 5c. This causes the device to reach higher, permanent resistance states. As the applied voltage increases beyond ~3 V (Fig. 5d), the increased localized Joule heating creates a higher concentration of TiO_x clusters all over the switching layer, where permanent filamentary paths are formed, likely stabilized by oxygen vacancies and altered surface terminations. Hence, this change in morphology and surface chemistry locks the device into distinct resistive states, where resistance states are retained even after power is removed.

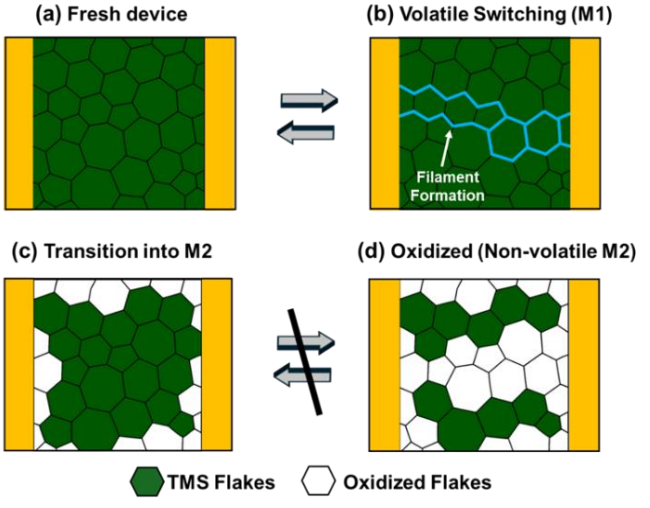

Fig. 5: Schematic illustration of the proposed switching mechanism in the prepared PMX-device (top view). (a-b) At low bias (Mode 1), reversible filament formation and rupture lead to volatile switching with self-resetting behavior. (c) Around ~2 V, edge-site oxidation and structural distortion mark the onset of a transition regime. (d) Higher bias voltage (~3 V), induces permanent filament formation and enables non-volatile switching.

To investigate the effect of electrical bias on the chemical stability of the 2D-TMS switching layer, compositional elemental mapping was performed on both freshly fabricated devices (low voltage operation, PMX_{M1}) and devices subjected to a 3 V stress (high voltage operation, PMX_{M2}). Fig. 6a and 6b show SEM-EDX mapping of the TMS channels in both devices PMX_{M1} and PMX_{M2} after electrical stimulation was applied. Elemental maps (Fig. 6a (i–iv), 6b (i–iv)) highlight the spatial distribution of Au, Ti, C, and O in the respective devices PMX_{M1} and PMX_{M2}. The PMX_{M1} device displayed uniform Ti and C signals with relatively lower oxygen content, indicating a negligible oxidized surface. In contrast, the stressed device PMX_{M2} showed a noticeable increase in oxygen signal intensity and redistribution, suggesting the surface modification due to oxidation. To cross-verify the EDX findings regarding surface chemistry and chemical changes in the materials, X-ray photoelectron spectroscopy (XPS) was carried out on both devices after being used. Full survey spectra (Fig. S4 and S5) confirmed the presence of Ti, C, O, and F in the corresponding devices PMX_{M1} and PMX_{M2}, consistent with the expected

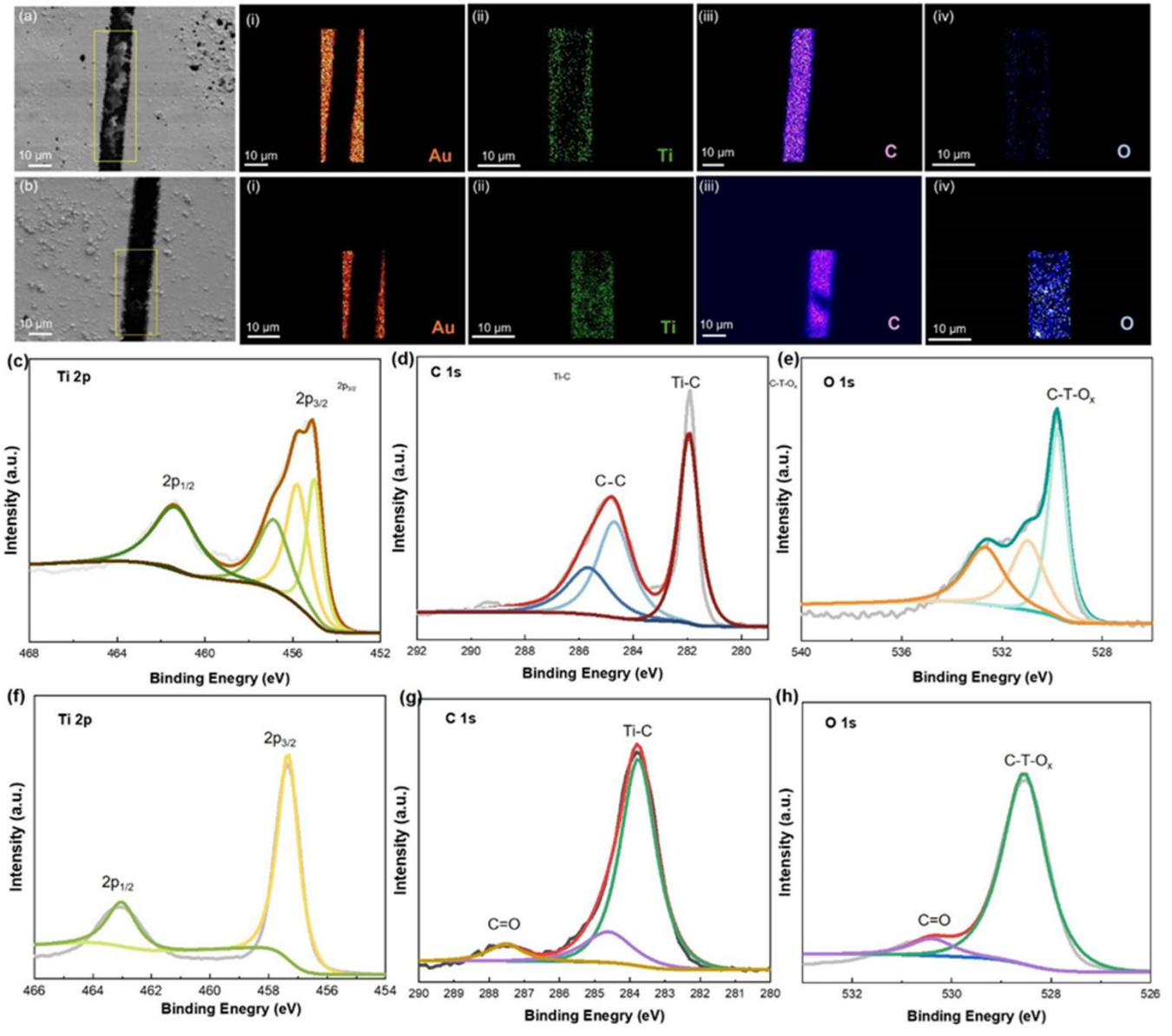

Fig. 6: Compositional and chemical analysis of PMX-memristor device under different operating voltages (M1 and M2): (a–b) SEM images of the TMS channel in (a) fresh (<2V) and (b) stressed (3 V) devices, insets are the corresponding EDX elemental maps for (i) Au, (ii) Ti, (iii) C, and (iv) O. (c-e) XPS spectra of fresh device shows (c) Ti 2p , (d) C 1s, and (e) O 1s. (f-h) XPS spectra after 3 V operation revealing (f) Ti 2p, (g) C1s, and (h) O 1s, indicates irreversible chemical transformation of the TMS active layer.

composition of delaminated TMS. However, comparative analysis revealed significant chemical evolution between the two states, confirmed the voltage-triggered structural changes. High-resolution XPS analysis (Fig. 6c-h) provides further insight into the underlying chemical transformations. In the PMX_{M1} device, the Ti 2p spectrum exhibited distinct peaks at 455.1 eV (Ti $2p_{3/2}$) and 461.5 eV (Ti $2p_{1/2}$), characteristic of Ti–C bonding, along with fitted peaks at 455.7 eV and 456.9 eV attributed to Ti^{2+} and Ti^{3+} states, respectively.[33] These features indicated that the TMS structure remained largely intact with negligible surface oxidation. The C 1s region (Fig. 6d) showed peaks at 282 eV, 284.7 eV and 285.7 eV, attributed to C–Ti–T_x, graphitic C–C, and CH_x/CO bonds, respectively. While the O 1s spectrum (Fig. 6e) showed peak signals at 529.8 eV, 531 eV, and 532.7 eV, associated with lattice-bound oxygen (C–Ti–O_x), hydroxyls, and minor C=O groups, typical of minimally oxidized, functionalized TMS surfaces. In contrast, the high-voltage device PMX_{M2} showed significant changes. The Ti 2p spectrum (Fig. 6f) shifted toward higher binding energies, with dominant peaks at ~457.3 and 463.1 eV, corresponding to Ti^{4+} states commonly found in TiO_2.[34,35] These changes confirmed that high-voltage operation induced significant oxidation, transforming conductive Ti–C bonds into insulating Ti–O structures. The corresponding C 1s spectrum (Fig. 6g) showed a notable decrease in the C–Ti signal and the emergence of a weaker peak near ~287.6 eV, indicating the formation of oxygen-containing carbon species such as carbonyl (C=O) or carboxyl groups, which indicates the structural degradation and oxidation.

Additionally, the O 1s spectrum (Fig. 6h) becomes more

Table 1: Comparison of recently reported MXene-based memristive devices that utilize single component MXene functional layers with the current work.

Structure	Architecture	Analog Switching	Switching Voltage	Switching Behavior	R_{ON}/R_{OFF}	Flexibility	Ref
Ag/V_2C/W	Sandwich	No	3.1V/1.2V	Volatile	NA	No	[37]
Ag/V_2C/W	Sandwich	No	4V/0.78V	Volatile and Non-Volatile	NA	No	[38]
Ag/V_2C/W	Sandwich	No	6 to 8V	Non-Volatile	10^4	No	[39]
Ag/$Ti_3C_2T_x$/Pt	Sandwich	No	3.3 V	Volatile and Non-Volatile	10^6	No	[40]
Cu/ Ti_3C_2/Cu/SiO_2/Si	Sandwich	No	0.68/-0.61	Volatile	NA	No	[41]
Al/$Ti_3C_2T_x$ /Pt	Sandwich	No	2.5 V/-2.3	Non-Volatile	10^3	No	[42]
Ag/$Ti_3C_2T_x$ /Pt	Sandwich	No	2.5V	Non-Volatile	10^4	No	[25]
Pt/$Ti_3C_2T_x$/ITO/Si	Sandwich	No	1.95V/-2.04V	Non-Volatile	10^2	No	[43]
rGO/FE- $Ti_3C_2T_x$ /rGO	Sandwich	No	2.8V/-1.6V	Volatile and Non-Volatile	103	Yes	[24]
Au/$Ti_3C_2T_x$/Au	Planar	Yes (Multistate from 0.5V to 4V)	~2V	Volatile and Non-Volatile	50	Yes	This work

intense, with a dominant peak shifted to ~529.9 eV, characteristic of lattice oxygen in TiO_2,[36] and a reduced intensity of higher binding energy components around 532.0 eV, which reflected the breakdown of surface hydroxyls and adsorbed species. Collectively, these XPS results confirmed a clear transformation from a carbide-rich, surface-functionalized TMS in the PMX_{M1} device to a partially oxidized, TiO_2-like structure PMX_{M2} device. This voltage-induced chemical transformation directly correlates with the device switching behavior, where low-voltage operation preserves the integrity of the 2D TMS network, enabling volatile and fully reversible memory states, while high-voltage bias triggers localized oxidation and defect formation, leading to the stabilization of conductive filaments and a transition to non-volatile switching behavior. These findings suggest that both device reliability and switching mode can be dynamically tuned by controlling operating voltage for desired volatile behavior ideal for synaptic emulation and sensing, or non-volatile operation suitable for memory storage.

Table 1 presents a comparative analysis of recently reported MXene-based memristive devices that utilize single-component MXene as a functional layer, providing a direct benchmark of the present device against the reported state-of-the-art. The fabricated PMX-memristor provides true analog switching with eight well-separated conductance states that can be incrementally written and read with biases below 4 V. Such fine-grained weight control is essential for high-accuracy neuromorphic hardware and is still uncommon in MXene devices, where most reports remain binary. In addition, the PMX-memristor exhibited voltage-controlled dual-mode volatile/ non-volatile switching behavior in a single MXene-based device. This tunability enables transient synaptic emulation and long-term memory storage, making it highly versatile for adaptive computing, real-time signal processing, and multifunctional sensing applications. Moreover, unlike conventional vertical MIM designs, our lateral structure provides direct surface access, enabling in situ characterization and functionalization, crucial for bio-sensing applications. It also simplifies fabrication, supports CMOS and microfluidic integration, and preserves key features for neuromorphic and resistive memory use, offering multifunctionality beyond what vertical stack architecture can achieve. Also, utilizing the flexibility of the substrate, mechanical pliability confirmed through repeated bending test positions the device for wearable neuromorphic processors, skin conformal sensors, and other applications that cannot accommodate rigid chips. Collectively, the analog precision, voltage tunability, surface accessibility, and mechanical flexibility deliver a set of functionalities not previously achieved in MXene-based memristor platforms. Compared to other planar 2D material-based memristors, such as those using CNTs[28] and a graphene-based analog resistive memory,[29] our PMX memristor device demonstrated comparable multistate performance while operating at significantly lower switching voltages. Notably, it uniquely supports voltage-tunable dual-mode behavior (volatile and non-volatile), a functionality absent in previous planar architectures. Together, these comparisons underscore the performance advantages of the presented device relative to both existing MXene-based memristors and other planar 2D material systems, highlighting their strong potential for compact, energy-efficient, and reconfigurable neuromorphic systems.

3.4 Spiking neural inference leveraging multi-state capability

The proposed device is demonstrated on two convolutional Spiking Neural Networks (SNNs) for the classification of the N-MNIST[44] and IBM's DVS128 Gesture[45] datasets. The networks were trained using the SLAYER framework[46] with a variation of the backpropagation algorithm based on the probability of a spiking neuron to change its state, that is, fire

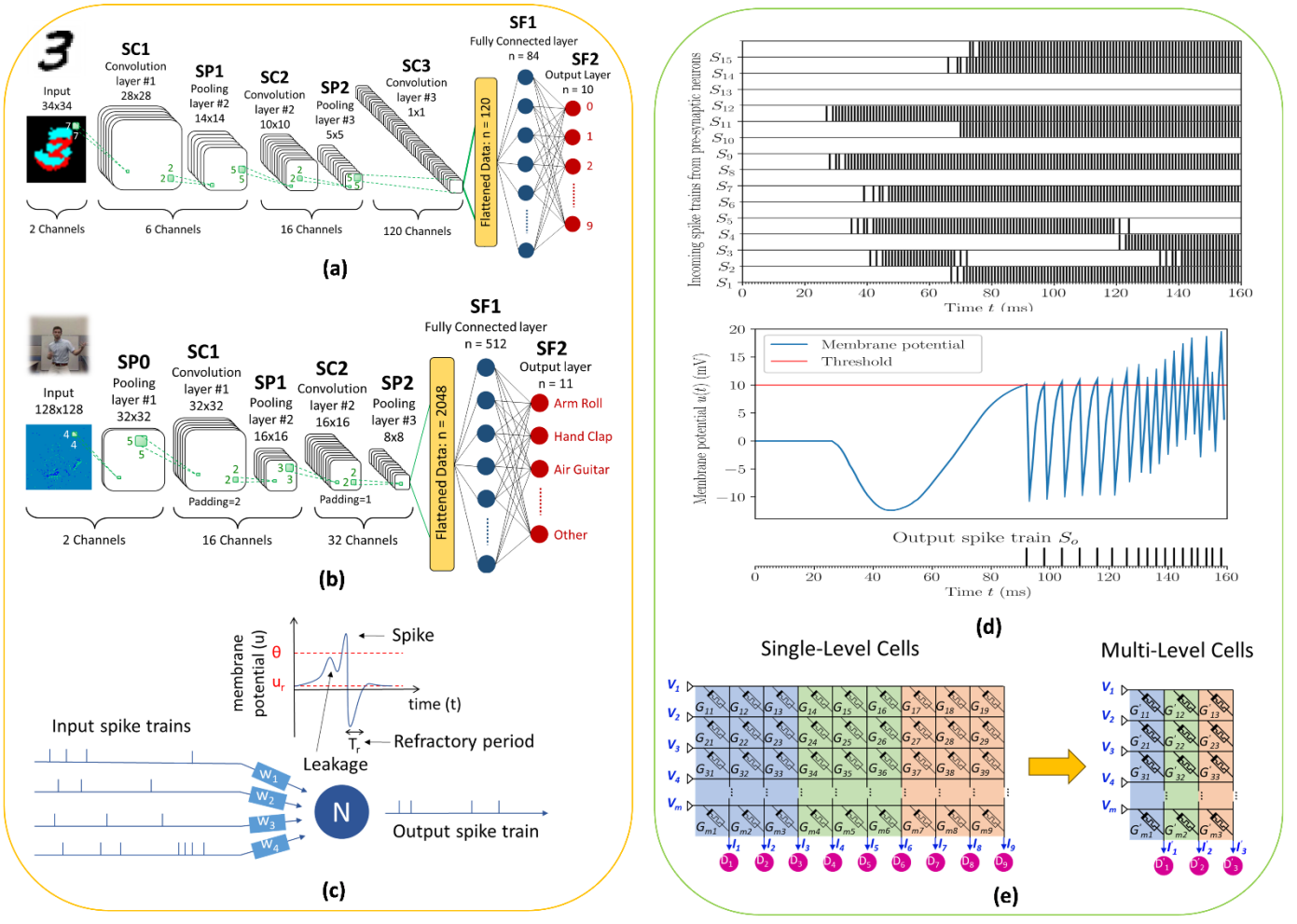

Fig. 7: Memristor-based implementation for SNN applications. (a) The N-MNIST SNN architecture, (b) the DVS128 Gesture SNN architecture, (c) operation of an SRM spiking neuron, (d) closeup of an SRM neuron's membrane potential and output over time during integration of incoming spike trains from preceding neurons, (e) an example of compacting a memristor-based crossbar array with single-level cells (left) after replacing with multi-level cells with 8 conductance states (right).

a spike or not. The winning class of each input sample is decided after the spiking neuron that was triggered the most at the output layer, *i.e.*, produced the highest number of spikes.

The input to SNNs needs to be in a spiking form as well, *i.e.*, the network is fed with a continuous-time event flow instead of static frames. A way to achieve this is with a neuromorphic camera, also known as a Dynamic Vision Sensor (DVS). A DVS resembles the retina of the human eye and is composed of pixel-neurons that react to changes in brightness. When a sufficient change has occurred to the brightness of a pixel-neuron, it generates a positive or negative event, depending on the polarity of the change. Examples of neuromorphic images are shown in Fig. 7a-b at the input of the SNNs for a single time instance. Blue colored pixels signify a positive event, while a negative one is denoted with red or green color, respectively. If there is no change, then the corresponding pixel-neurons remain silent (black/light blue pixels).

The N-MNIST dataset is a neuromorphic, *i.e.*, spiking, version of the MNIST dataset, which comprises images of handwritten arithmetic digits in gray-scale format.[44] It consists of 70000 sample images that are generated from the saccadic motion of a DVS in front of the original images in the MNIST dataset. The samples in the N-MNIST dataset have a duration of 300 ms. The SNN architecture, shown in Fig. 7a, is a spiking version of the LeNet-5 architecture.[47] It consists of 3 convolutional layers with two 2x2 sum-pooling layers in between them and two fully connected layers at the end for the final decision of the network. The classification accuracy on the testing set is 97.8%.

IBM's DVS128 Gesture dataset consists of 29 individuals performing 11 hand and arm gestures in front of a DVS, such as hand waving and air guitar, under 3 different lighting conditions.[45] In total, the dataset comprises 1342 samples of duration 6 s, which is trimmed to 1.5 s to speed up the simulation. The designed SNN, shown in Fig. 7b, starts with a 4x4 sum-pooling layer to reduce the size of the input samples. Next, there are two convolutional layers followed by a 2x2 sum-pooling layer each. The architecture is concluded with two fully connected layers. The network performs with 86.4% accuracy on the testing set, which is acceptable considering the shortened samples of the dataset and the shallower

architecture compared to the original one proposed in IBM's DVS128 Gesture datasets.

Both networks employ the Spike Response Model (SRM) for their neurons, which is a generalized version of the Integrate and Fire (I&F) model.[48,49] Its operation is illustrated in Fig. 7c. In the SRM, the state of a neuron at any given time is described by its membrane potential u. At its resting state, the membrane potential is set to a low value u_{rest}. The neuron integrates the incoming spikes from the synapses at its input, and the membrane potential is increased or decreased according to the spike polarity. Once the potential reaches a certain threshold θ, the neuron fires a spike, which is propagated to the next layer of neurons via the synapses connected to its output, and the neuron is reset to its resting state. At the same time, the neuron is regulated to not fire again for a while. The minimum time in-between successive spikes is called the refractory period. Fig. 7d presents a close-up of the membrane potential over time while spike trains arrive at its input from preceding neurons. To mathematically express the above functionality, the SRM considers that the action of a neuron at any given time is a response to both the incoming activity and the neuron's own output. For this purpose, two response functions are used, namely, the synaptic kernel ε and the refractory kernel η. Eq. 1 expresses the membrane potential u of an SRM neuron:[50]

$$u(t) = \sum_i \omega_i (\varepsilon * S_i)(t) + (\eta * S_o)(t) + u_{rest} \quad (1)$$

where ω_i is the weight of the synapse driving the i^{th} neuron input, $*$ denotes the convolution product, S_i and S_o are the input and output spike trains of the neuron, respectively.

The synaptic weights of the networks are quantized in a 9-bit integer representation, which are then mapped on the proposed memristive devices arranged in multiple crossbar arrays. Each weight occupies 3x3-bit devices, as each device is operated in $2^3 = 8$ different conductance states. Shown in Fig. 7e, the size of a crossbar array is reduced by 3x compared to the case when using binary devices, *i.e.*, 2^1 conductance states, resulting in higher compactness and lower circuit area. Once the synaptic weights are written on the crossbar arrays, inputs $V_1, V_2, \dots, V_m$ are applied on the corresponding word lines and are shared by all memory cells in the same row. The current I_{ij} passing through a cell c_{ij}, that connects row i to column j, is the product of the input voltage V_i and the cell's conductivity G_{ij}, or $I_{ij} = V_i \cdot G_{ij}$. According to Kirchhoff's law, the total output current emerging bit line j is equal to the sum of all cell currents across the column, or $I_j = \sum_i V_i \cdot G_{ij}$, which is equivalent to the dot product operation.

Finally, in our experiments, we performed a complete inference on the testing sets of the two case studies. Regarding the N-MNIST SNN, the average read energy consumption per spike is 64 nJ, while the larger Gesture SNN, *i.e.*, containing more synaptic weights and accepting longer input samples, consumes an average of 127 nJ per spike. These energy figures fall well within the efficient operational range reported for neuromorphic systems, highlighting the suitability of our devices for scalable, low-power neuromorphic computing on resource-constrained edge platforms.

4. Conclusion

We report the first planar $Ti_3C_2T_x$ MXene-based memristor by a facile, scalable spin-coating and photolithographic process on a cyclic-olefin-copolymer substrate. The prepared device features a voltage-controlled transition between volatile and non-volatile regimes. Electrical characterization shows a voltage-controlled dual mode: self-resetting, volatile switching below about 2 V and stable, non-volatile storage above about 3 V, with eight well-separated resistance levels. Correlated SEM-EDX and XPS mapping before and after high-bias stress reveals a bias-induced $Ti \rightarrow TiO_x$ transformation that anchors conductive filaments, explaining the transition from transient to permanent conductance states and underscoring the value of the open layout for in-situ mechanistic studies. Harnessing the eight conductance levels, we quantized synaptic weights to 9 bits and implemented them in 3 × 3 device groups inside crossbar arrays, shrinking the array footprint three-fold relative to binary cells. Hardware-based inference on two benchmark spiking neural-network tasks delivered 97.8% accuracy on N-MNIST and 86.4% on DVS-Gesture, with read energies of only 64-127 nJ per spike. The results identify this planar platform as a promising candidate for next-generation flexible, neuromorphic, and multifunctional memory systems. Future efforts will focus on integrating larger crossbar arrays and dynamic learning behaviors to enhance the functionality of planar MXene-based neuromorphic hardware and enable applications in smart biosensing.

Conflicts of Interest

There is no conflict to declare.

Supporting Information

Applicable.

CRediT Statement

Rami Homsi: Writing - Original draft, Methodology, Investigation, Validation, Visualization. **Shoaib Anwer:** Writing - Review & editing, Investigation, Visualization. **Heba Abunahla:** Conceptualization Methodology, Supervision, Writing - Review & editing. **Theofilos Spyrou:** Writing - Original draft, Software, Visualization, Data curation. **Rajendra Bishnoi:** Supervision. **Said Hamdioui:** Supervision. **Baker Mohammad:** Project administration, Funding acquisition, Supervision, Resources. **Anas Alazzam:** Conceptualization, Writing - Review & editing, Project administration, Supervision, Resources.

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